AMENDMENTS TO THE CLAIMS

Claims 1-43 (cancelled).

44. (original) An integrated circuit device prepared by a process

comprising:

forming a first layer containing a chalcogenide material;

forming a second layer over the first layer wherein the second layer is formed of at least one non-chalcogenide chemical element;

forming a third layer over the second layer; and

diffusing the second layer into the first layer to create an integral layer including

materials from the first and second layers, wherein the material from the second layer

comprises at least the non-chalcogenide chemical element.

45. (Original) The chalcogenide integrated circuit according to claim 44, wherein diffusing to create the integral layer includes irradiating the second layer through the third layer such that the second layer is diffused into the first layer.

46. (Original) The chalcogenide integrated circuit according to claim 45, wherein irradiating includes exposing the second layer to ultra-violet light.

47. (Original) The chalcogenide integrated circuit according to claim 44, wherein the steps are performed in the recited order.

48. (Original) A chalcogenide integrated circuit device prepared by a process comprising:

forming a first layer;

forming a second layer on the first layer;

forming a third layer on the second layer, wherein the third layer is essentially transparent to irradiation; and

irradiating the second layer through the third layer to cause the second layer to diffuse into the first layer thereby creating an integral layer of materials from the first and second layers.

49. (original) A chalcogenide integrated circuit device prepared by a process comprising:

forming a chalcogenide layer;

forming a metal layer over the chalcogenide layer;

forming a barrier layer over the metal layer; and

irradiating the metal layer through the barrier layer to diffuse the metal layer into the chalcogenide layer to create a metal doped chalcogenide layer.

50. (Original) A chalcogenide integrated circuit device prepared by a process comprising:

forming a formative GeSe layer;

forming a silver layer on the formative GeSe layer;

forming a thin barrier layer on the silver layer;

irradiating the silver layer through the thin barrier layer to diffuse the silver layer into the formative GeSe layer to create the doped chalcogenide layer.

Claims 51-123 (cancelled).

124. (Original) The integrated circuit according to claim 44 wherein the second layer comprises a metal.

125. (Original) The integrated circuit according to claim 124 wherein the second layer comprises silver.

126. (Original) The integrated circuit according to claim 44 wherein the third layer comprises a chalcogenide material.

127. (Original) The integrated circuit according to claim 126 wherein the third layer comprises germanium-selenide.

128. (Original) The integrated circuit according to claim 44 wherein the integral layer comprises silver.

129. (Original) The integrated circuit according to claim 44 wherein the integral layer comprises silver-germanium-selenide.

130. (Original) The integrated circuit according to claim 44 wherein the third layer is formed to a thickness in a range of about 20Å to about 50Å.

131. (Original) The integrated circuit according to claim 130 wherein the first layer comprises germanium-selenide.

132. (Original) The integrated circuit according to claim 44 wherein the third layer is a barrier layer.

133. (Original) The integrated circuit according to claim 132 wherein the barrier layer reduces agglomeration from the second layer.

134. (Original) The chalcogenide integrated circuit according to claim 49 wherein the chalcogenide layer comprises germanium-selenide.

135. (Original) The chalcogenide integrated circuit according to claim 49 wherein the metal layer comprises silver.

136. (Original) The chalcogenide integrated circuit according to claim 49 wherein the metal layer is formed to a thickness in a range of about 100Å to about 200Å.

137. (Original) The chalcogenide integrated circuit according to claim 49 wherein the barrier layer comprises a material transparent to light.

138. (Original) The chalcogenide integrated circuit according to claim 49 wherein the barrier layer is essentially transparent to an energy source for driving the metal layer into the chalcogenide layer.

139. (Original) The chalcogenide integrated circuit according to claim 49 wherein the barrier layer comprises a chalcogenide material.

140. (Original) The chalcogenide integrated circuit according to claim 139 wherein the barrier layer comprises germanium-selenide.

141. (Original) The chalcogenide integrated circuit according to claim 49 wherein the barrier layer is formed of a material which is the same as the chalcogenide layer.

142. (Original) The chalcogenide integrated circuit according to claim 49 wherein the barrier layer reduces agglomeration from the metal layer.

143. (Original) The chalcogenide integrated circuit according to claim 49 wherein the barrier layer is formed to a thickness in a range of about 20Å to about 50Å.

144. (Original) The chalcogenide integrated circuit according to claim 49 wherein the barrier layer has a thickness of about 30Å.

145. (Original) The chalcogenide integrated circuit according to claim 49 wherein the chalcogenide layer has a thickness in a range of about 500Å to about 1000Å.